

CLAIMS

What is claimed is:

- 1 1. An integrated circuit fabricated on a chip, comprising:
2 an on-chip logic analyzer including timestamp logic;
3 an on-chip memory capable of storing data selected by said on-chip logic analyzer;
4 wherein the data stored by said on-chip memory is combined with a timestamp field
5 representing the number of cycles since the previous store operation.
- 1 2. The system of claim 1, wherein the timestamp logic includes a timestamp counter that
2 generates a timestamp count value signal indicating the number of clock cycles since the previous
3 store operation.
- 1 3. The system of claim 2, wherein the on-chip logic analyzer generates a store signal when
2 data is to be stored in the memory, and wherein the timestamp counter receives the store signal and
3 resets the timestamp count value.
- 1 4. The system of claim 3, wherein the on-chip logic analyzer comprises data selection logic
2 that selects data to be stored, and which generates the store signal.
- 1 5. The system of claim 3, wherein the timestamp count value signal is encoded in n bits which
2 is stored as the timestamp field together with the stored data, thereby storing one of x timestamp
3 codes with the stored data, where $x = 2^n$.

1 6. The system of claim 5, wherein the number of valid timestamp count values y is less than
2 the number of timestamp codes x .

1 7. The system of claim 5, wherein the number of bits n used to encode the timestamp count
2 value is 8 or less.

1 8. The system of claim 5, wherein the number of bits n used to encode the timestamp count
2 value comprises less than 20% of the available bits in each memory entry.

1 9. The system of claim 5, wherein the number of bits n used to encode the timestamp count
2 value comprises less than 15% of the available bits in each memory entry.

1 10. The system of claim 5, wherein the number of bits n used to encode the timestamp count
2 value comprises less than 12.5% of the available bits in each memory entry.

1 11. The system of claim 5, wherein the timestamp counter forces a store operation when the
2 timestamp count value reaches a predetermined value.

1 12. The system of claim 11, wherein the timestamp counter generates the store signal when the
2 timestamp count value reaches the predetermined value, and wherein said timestamp counter is
3 reset in response.

1 13. The system of claim 12, wherein a timestamp value greater than the predetermined value
2 represents that the data stored is invalid.

1 14. The system of claim 3, wherein the timestamp logic further includes a multiplexer coupled
2 to said memory, and wherein said multiplexer receives the timestamp count value signal at one
3 input terminal, and selects the timestamp count value signal for storing in said memory in response
4 to the assertion of a timestamp enable signal.

1 15. The system of claim 14, wherein the multiplexer receives additional data bits at a second
2 input terminal, and wherein said multiplexer selects the additional data bits for storing in said
3 memory if said timestamp enable signal is de-asserted.

1 16. A system for storing timestamp information together with selected data, comprising:
2 a memory device with multiple entries capable of storing a bit field of a predetermined
3 length;
4 data selection logic that monitors data, and which selectively stores data to said memory;
5 a timestamp counter coupled to said memory for supplying a timestamp value which can be
6 selectively stored with said data in said memory;
7 wherein said timestamp value represents the number of clock cycles that have been counted
8 by said timestamp counter since the previous entry was stored in said memory, and wherein said
9 timestamp counter forces a store operation if the timestamp value reaches a predetermined value.

1 17. The system of claim 16, further comprising a multiplexer coupled to said memory, and
2 wherein said multiplexer receives the timestamp value at one input terminal, and selects the
3 timestamp count value signal for storing in said memory in response to the assertion of a
4 timestamp enable signal.

1 18. The system of claim 17, wherein the data is stored in a bits in a memory entry, and the
2 timestamp value is stored in x bits in memory, and wherein the number of data bits a stored in
3 memory is substantially greater than the number of timestamp value bits n stored in memory.

1 19. The system of claim 17, wherein the multiplexer receives additional data bits of width n at
2 a second input terminal, and wherein said multiplexer selects the additional data bits for storing in
3 said memory if said timestamp enable signal is de-asserted.

1 20. The system of claim 19, wherein the timestamp counter comprises an n bit digital counter
2 that is reset each time data is stored in said memory.

1 21. The system of claim 20, wherein the clock cycles occur at a frequency in excess of 1 GHz.

1 22. The system of claim 20, wherein the clock cycles occur at a frequency in excess of 800
2 MHz.

1 23. The system of claim 20, wherein the clock cycles occur at a frequency in excess of 600
2 MHz.

1 24. The system of claim 20, wherein the clock cycles occur at a frequency in excess of 400
2 MHz.

1 25. The system of claim 20, wherein the number of possible timestamp count values x , where x
2 $= 2^n - 1$, is less than the number of cycles that may occur between store operations.

1 26. The system of claim 20, wherein the number of bits n used to encode the timestamp count
2 value is 8 or less.

1 27. The system of claim 20, wherein the number of bits n used to encode the timestamp count
2 value comprises less than 20% of the available bits in each memory entry.

1 28. The system of claim 20, wherein the number of bits n used to encode the timestamp count
2 value comprises less than 15% of the available bits in each memory entry.

1 29. The system of claim 20, wherein the number of bits n used to encode the timestamp count
2 value comprises less than 12.5% of the available bits in each memory entry.

1 30. The system of claim 20, wherein the timestamp counter, data selection logic, and memory
2 are provided as part of an integrated circuit.

31. A processor fabricated on a chip, comprising:

an on-chip logic analyzer including a timestamp counter;

an on-chip memory capable of storing data selected by said on-chip logic analyzer, said memory having a width of z bits;

wherein said timestamp counter counts the number of clock cycles since the previous data storage, and generates a timestamp count value of n bits, which can be selectively stored with said data in said memory, and wherein said timestamp counter is capable of forcing storage of data when the timestamp count value reaches a predetermined value.

32. The processor of claim 31, wherein the selective storage of the timestamp count value in the memory is controlled by a timestamp enable signal.

33. The processor of claim 31, wherein the memory stores the n bits representing the timestamp count value, together with y bits of stored data, when the timestamp enable signal is asserted, and wherein the number of bits y equals $z - n$.

34. The processor of claim 33, wherein the memory stores w bits of data when the timestamp enable signal is not asserted, and wherein the number of bits w equals z .

35. The processor of claim 31, wherein the data that is stored when the timestamp counter reaches a value greater than the predetermined value is invalid.